

Fig. 9.28 Fast reset circuit for inverting-type peak detectors.

switches. If fast resetting is needed, C_1 and the ON resistance of SW_1 must be as small as practical. Another method of implementing the HOLD mode is to place a switch in series with the input signal to "gate" it to OFF. When only the PEAK DETECT and RESET modes are needed, switch SW_1 can be eliminated if SW_2 has very low impedance such as that of relay contacts. Figure 9.28 shows a very fast method for resetting the inverting-type peak detectors with a current-gain sample-and-hold switch. (See Sec. 9.4.)

This circuit has the advantage that the switch in series with D_1 is not necessary since the sample-and-hold switch has very low output impedance. To reset C_1 to 0 V, V_{reset} must be zero. Capacitor C_1 can be reset to $+10$ V by making V_{reset} equal to -10 V so that input peaks can be detected over the full -10 to $+10$ V range.

9.4.5 Peak-to-peak detector Figure 9.29a shows a method for measuring the peak-to-peak value of a signal that swings both positive and negative in amplitude. If only positive peak detectors are available, the circuit can be built using one extra amplifier as shown in Fig. 9.29b.

9.6 Comparators

Comparators are used as analog/digital (hybrid) building blocks, since the digital output signal is simply the answer to the question: Is the analog input signal greater than or less than the analog reference signal? The input and reference signals can come from voltage or current sources or from a combination of the two types of sources. When operational amplifiers are used as comparators, there are usually one or more summing resistors connected to the inverting input (summing junction) of the operational amplifier. One can think of the circuit as comparing currents

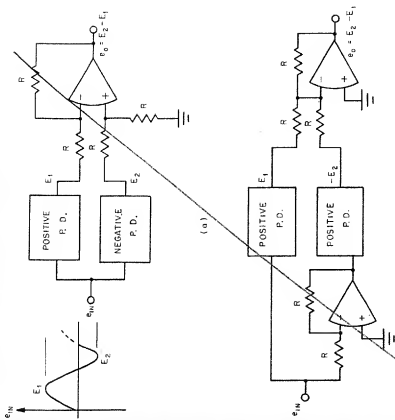


Fig. 9.29 Peak-to-peak detector circuits: (a) using one positive and one negative peak detector; (b) using two positive peak detectors.

of voltages. In this section we shall consider several types of such comparators.

9.6.1 Zero-crossing detector The simplest comparator is the zero-crossing detector which answers the question: Is the input signal greater than or less than zero? A typical circuit for such a detector is shown in Fig. 9.30. The limit circuit shown in the figure produces one output level when i_1 is positive and a different output level when i_1 is negative. Since the limit circuit changes state when i_1 changes sign, the comparison point occurs when $i_1 = 0$ as shown below (assume the summing junction potential is zero):

$$i_1 = i_3 + i_2 \quad (9-2)$$

$$\frac{e_1}{R} = i_3 + i_2 \quad (9-3)$$

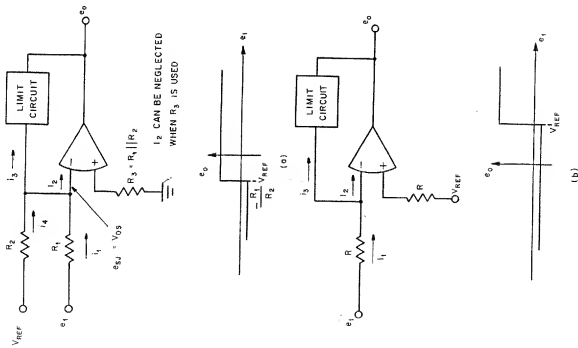


Fig. 9.31 Two-level detector circuits: (a) summing type; (b) differential type.

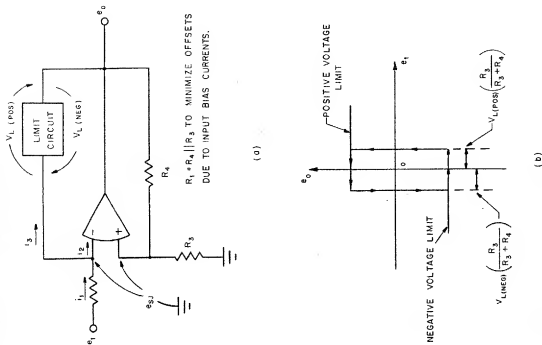


Fig. 9.32 Zero-crossing detector with hysteresis. (a) Circuit diagram; (b) transfer curve.

but

$$e_o = e_{sz} \pm V_L$$

Thus

$$e_{sz} = \pm V_L \frac{R_3}{R_3 + R_4} \quad (\text{hysteresis})$$

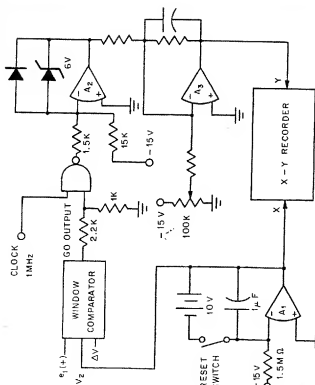


Fig. 9.34 Probability density analyzer.

When the input signal drops to a value below the window, the LOW output will switch to a logical 1 and the GO output will drop to a logical 0. When the input signal exceeds the window, the HIGH output will be at a logical 1 and the other outputs at a logical 0.

The window comparator is shown in Fig. 9.34 as part of a probability density analyzer. The GO output of the window comparator goes to HIGH each time the input signal is inside the window. When the clock is HIGH, the GO output are both HIGH, the output of the first NAND goes to LOW. A_2 is a comparator that is used to generate precision voltage levels for the RC averaging filter. The 100 k Ω potentiometer is adjusted to null the offset, since the LOW output of A_2 is not 0 V. A_1 is connected as an integrator that sweeps the window center from -10 to $+10$ V at a rate of 1 V/s. The window width, ($2 \Delta V$) and the rate the window is swept by is a function of the input being analyzed.

9.6.6.4 Amplitude classifier

9.6.4 Amplitude classifier Often it is required to sort items into many different bins. An example of this is grading apples into different groups according to size. Figure 9.35 shows how a system can be implemented

. , C TO ATTENUATE HIGH - FREQUENCY NOISE

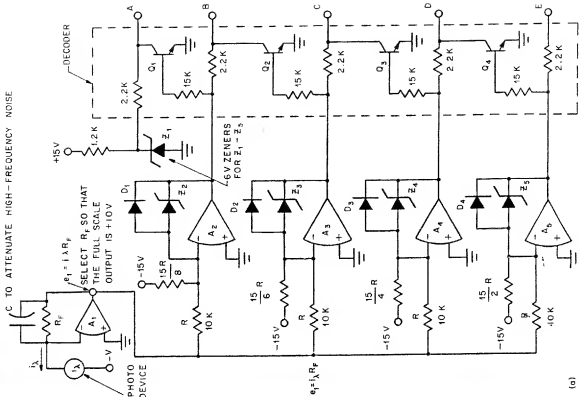


Fig. 9.35 Five-level amplitude classifier. (a) Circuit diagram.

OP AMP OUTPUTS		DECODER OUTPUTS				
		Z_1	A_2	A_3	A_4	A_5
$8 < e_1 \leq 10$		1	0	0	0	0
$6 < e_1 \leq 8$		1	1	0	0	0
$4 < e_1 \leq 6$		1	1	1	0	0
$2 < e_1 \leq 4$		1	1	1	1	0
$0 \leq e_1 \leq 2$		1	1	1	1	1

FOR OPERATIONAL AMPLIFIER		DECODER OUTPUTS				
		A	B	C	D	E
LOGICAL 1 = 6 V		1	0	0	0	0
LOGICAL 0 = .6V		0	1	0	0	0
		0	0	1	0	0
		0	0	0	1	0
		0	0	0	0	1

Fig. 9.35 (b) Table of output codes.

by using operational amplifiers as comparators. Amplifier A_1 operates as a current-to-voltage converter for the light-sensitive photodiode array which is used to detect the size of the apertures. Amplifiers A_2 to A_5 operate as biased comparators with a simple clamp circuit. The decoder ensures that only one logic output is at HIGH at a time. This decoder can drive TTL (transistor-transistor logic) or DTL (diode-transistor logic) directly or an n-p-n switching transistor which can control larger currents such as the coil current of a relay. Hysteresis can be added to each of the comparators for noise immunity if desired.

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